IN THE CLAIMS:

The status of the claims is as follows:

1. (Original) A computer implemented method of modifying characteristics of a circuit, the method comprising:

determining a set of objective parameters for the circuit;

receiving noise constraints for the circuit; and

optimizing values of the objective parameters based on the noise constraints.

2. (Currently Amended) The method of claim 1 further including:

developing a set of sensitivity factors based on the objective parameters and timing constraints gates to meet ~~noise margins in accordance with~~ the noise constraints, ~~such that~~ the sensitivity factors characterizing ~~characterize~~ a noise sensitivity of the circuit;

selecting objective parameter values and modified noise margins based on the sensitivity factors, ~~such that~~ the objective parameter values minimizing ~~minimize~~ power costs to the circuit and meeting individual noise margins; and

repeating the developing and selecting until changes in the objective parameter values fall below a predetermined threshold.

3. (Currently Amended) The method of claim 2 further including:

allocating initial delay targets ~~noise margins~~ to a plurality of nodes in the circuit, the delay targets meeting the noise margins;

setting initial objective parameter values in accordance with the initial noise margins; and

repeating the allocating and setting for varied timing budgets ~~noise margins~~.

4. (Original) The method of claim 3 further including selecting discrete components of the objective parameters such that the objective parameter values define dynamic logic settings.

5. (Original) The method of claim 4 further including selecting one or more dynamic logic families, each dynamic logic family having dynamic gates with corresponding transistor widths and power levels.

6. (Original) The method of claim 3 further including selecting continuously tunable components of the objective parameters such that the objective parameter values define static logic settings.

7. (Original) The method of claim 6 further including selecting one or more static logic gates, each static logic gate having corresponding widths and power levels.

8. (Currently Amended) The method of claim 2, wherein the circuit has a plurality of nodes, the method further including:

measuring power costs to a full cone of logic behind each node in the circuit;

calculating power costs to a full cone of logic ahead of each node in the circuit;

summarizing the measured power costs and the calculated power costs into a common sensitivity parameter.

9. (Original) The method of claim 2 further including:

constructing an objective function based on the sensitivity factors; and

inputting the objective function to a linear program solver such that the linear program solver generates the objective parameter values and the noise margins.

10. (Original) The method of claim 1 further including:

receiving timing constraints for the circuit; and

optimizing the objective parameter values based on the timing constraints.

11. (Currently Amended) The method of claim 10 further including:

determining delay targets ~~timing margins~~ in accordance with the timing constraints~~;~~, said delay targets ~~timing margins~~ including minimum and maximum delays for a plurality of nodes in the circuit.

12. (Original) The method of claim 1 further including:

receiving physical constraints for the circuit; and

optimizing the objective parameter values based on the physical constraints.

13. (Original) The method of claim 1 further including:

conducting a topological analysis on critical paths of the circuit, where the optimized objective parameter values are used in the critical paths;

correcting the objective parameters and noise constraints for topological costs that are above a predetermined level; and

repeating the optimizing with the corrected objective parameters and noise constraints.

Claims 14-17 (Canceled).

18. (Currently Amended) A computer implemented method of optimizing values of objective parameters for a circuit, the method comprising:

developing a set of sensitivity factors based on the objective parameters and timing constraints to meet ~~noise margins in accordance with~~ noise constraints for the circuit, ~~such that~~ the sensitivity factors characterizing ~~characterize~~ a noise sensitivity of the circuit, the developing to include allocating initial delay targets to a plurality of nodes in the circuit, the delay targets to meet the noise constraints, setting initial objective parameter values in accordance with the noise constraints by selecting continuously tunable components of the objective parameter values, the initial objective parameter values to define static logic settings, and repeating the allocating and the setting for adjusted noise margins;

selecting objective parameter values and modified noise margins based on the sensitivity factors, ~~such that~~ the objective parameter values minimizing ~~minimize~~ power costs to the circuit; and

repeating the developing and the selecting until changes in the objective parameter values fall below a predetermined threshold.

19. (Canceled).

20. (Currently Amended) The method of claim 18 ~~19~~ further including selecting discrete components of the objective parameters such that the objective parameter values define dynamic logic settings.

21. (Original) The method of claim 20 further including selecting one or more dynamic logic families, each dynamic logic family having dynamic gates with corresponding transistor widths and power levels.

22. (Canceled.)

23. (Currently Amended) The method of claim 18 ~~22~~ further including selecting one or more static logic gates, each static logic gate having corresponding widths and power levels.

24. (Currently Amended) A computer-readable storage medium to store ~~storing~~ a set of instructions~~, the set of instructions~~ capable of being executed by a processor to perform a method of optimizing values of objective parameters for a circuit to~~, the method of comprising~~:

develop ~~developing~~ a set of sensitivity factors based on the objective parameters and timing constraints to ~~noise margins in accordance with~~ meet noise constraints for the circuit, ~~such that~~ the sensitivity factors to characterize ~~characterizing~~ a noise sensitivity of the circuit, the medium further including instructions to allocate initial delay targets to a plurality of nodes in the circuit, the delay targets to meet the noise constraints, set initial objective parameters values in accordance with the noise constraints by selecting continuously tunable components of the objective parameters, the initial objective parameter values to define static logic settings,~~;~~ and repeat the allocating and setting for adjusted delay targets;

select ~~selecting~~ objective parameter values and modified noise margins based on the sensitivity factors, ~~such that~~ the objective parameter values to minimize power costs to the circuit; and

repeat the developing and selecting until changes in the objective parameter values fall below a predetermined threshold.

25. (Canceled).

26. (Currently Amended) The medium of claim 24 ~~25~~ wherein the method further includes selecting discrete components of the objective parameters such that the objective parameter values define dynamic logic settings.

27. (Canceled).